PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LHF00L04

Flash Memory

8M (1MB × 8)

(Model No.: LHF00L04)

Spec No.: FM037006
Issue Date: June 18, 2003

SHARP

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To;

PRELIMINARY

SPECIFICATIONS

Product Type 8Mbit Flash Memory

LHF00L04

Model No. (LHF00L04)

This device specification is subject to change without notice.

* This specifications contains 38 pages including the cover and appendix.

CUSTOMERS ACCEPTANCE

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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

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- Office electronics
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- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

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- Mainframe computers
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- Rescue and security equipment
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- Medical equipment related to life support, etc.

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LHF00L04
8Mbit (1Mbit×8)
Firmware Hub Flash MEMORY

- Conforms to Intel LPC Interface Specification 1.1
- Optimized Array Blocking Architecture
  - Fifteen 64-KByte Uniform Blocks
  - Eight 8-KByte Boot Sectors
  - Boot Sector Data Protection for each 8-KByte sector
  - Full Chip Erase for A/A Mode Only
- V_{CC}=3.0V-3.6V Operation
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Low Power Consumption (FWH Interface)
  - Standby Current : 15µA (Max.)
  - Read Current : 15mA (Max.)
  - Erase or Program Current : 25mA (Max.)
- Erase or Program Operation
  - Byte Program Time : 25µs (Typ.)
  - Sector Erase Time : 0.6s (Typ.)
  - Block Erase Time : 1.2s (Typ.)
  - Full Chip Erase Time : 40s (Typ.)
  - Sector Rewrite Time : 0.8s (Typ.)
  - Block Rewrite Time : 2.8s (Typ.)
- Operating Temperature 0°C to +85°C
- CMOS Process (P-type silicon substrate)
- Two Operational Modes
  - Firmware Hub (FWH) Interface mode for In-System operation
  - Address/Address Multiplexed Interface (A/A) Mode for production erasing and programming
- FWH Interface Mode
  - 5 signal communication interface supporting byte Read and Write
  - 33MHz clock frequency operation
  - WP# and TBL# pins provide hardware data protection for entire chip and/or boot sector
  - Status Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - ID pins for multi-chip selection
- Multi Byte Read Mode (FWH)
  - Max. 128-Byte Sequential Read Operation for data transfer
- A/A Interface Mode
  - 11 pin multiplexed address and 8-pin data I/O interface
  - Supports fast In-System or PROM programming for manufacturing
- CMOS and PCI I/O Compatibility
- 40-Lead TSOP (Normal Bend)
- ETOX[TM*] Flash Technology
- Not designed or rated as radiation hardened

* ETOX is a trademark of Intel Corporation.

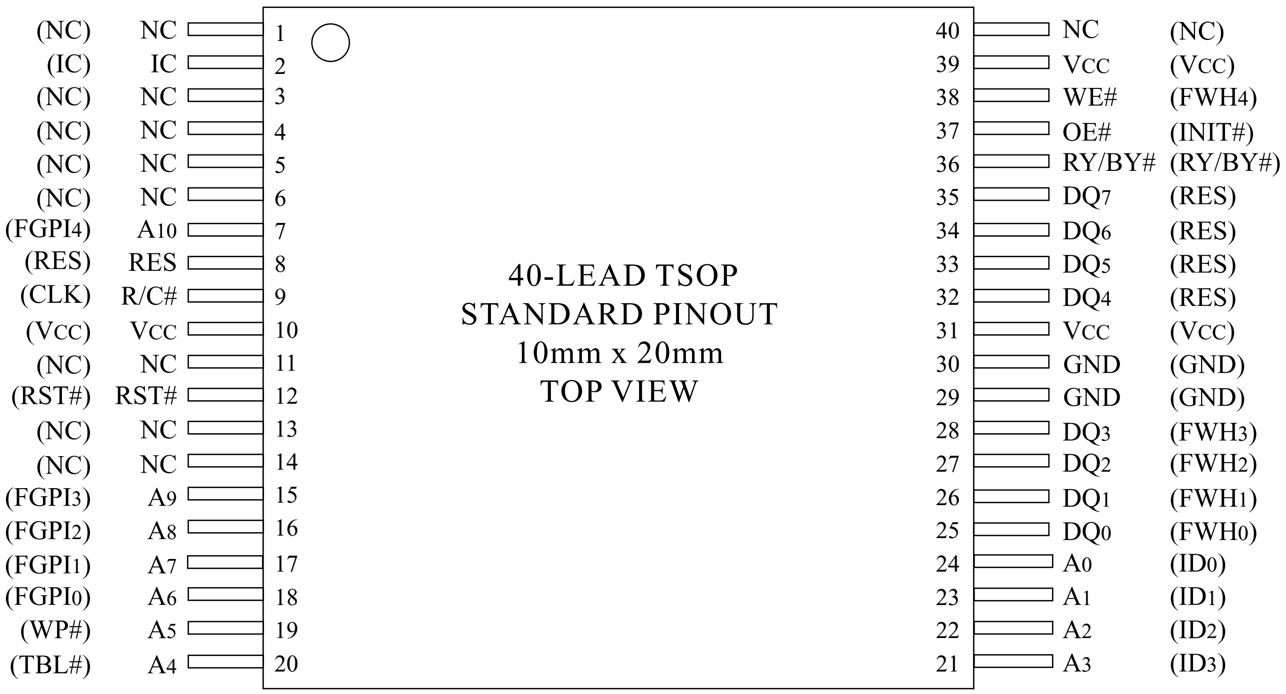


Figure 1. 40-Lead TSOP (Normal Bend) Pinout

Symbols inside ( ) are those for FWH mode.

1 Product Description

The product is offered in 40-Lead TSOP (Normal Bend) package. Refer to Figure 1 for pinouts and Table 1 for pin descriptions.

Table 1. Pin Descriptions

Symbol	Type	Interface		Name and Function
		A/A	FWH	
RST#	INPUT	O	O	RESET: When low (V_{IL}), RST# resets internal automation and inhibits erase and program operations, which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode.
IC	INPUT	O	O	INTERFACE CONFIGURATION: This pin determines which interface is operational. This pin must be held high (V_{IH}) for A/A mode and low (V_{IL}) for FWH mode. This pin is internally pulled-down with a resistor between 20KΩ-100KΩ.
INIT#	INPUT		O	INITIALIZE: This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited.
FWH_4	INPUT		O	FWH INPUT: To indicate start of a data transfer operation. This pin is also used to abort an FWH cycle in progress.
FWH_3-FWH_0	INPUT/ OUTPUT		O	FWH INPUTS/OUTPUTS: To provide FWH control signals, as well as addresses and command Inputs data/Outputs data.
CLK	INPUT		O	CLOCK: To provide a clock input to the control unit.
ID_3-ID_0	INPUT		O	IDENTIFICATION INPUTS: These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. These pins are internally pulled-down with a resistor between 20KΩ-100KΩ.
$FGPI_4$-$FGPI_0$	INPUT		O	GENERAL PURPOSE INPUTS: These individual inputs can be used for additional board flexibility. The state of these pins can be read through GPI registers.
TBL#	INPUT		O	TOP BOOT LOCK: When low, prevents erasing and programming to the boot sectors at top (highest address) of memory. When TBL# is high, it disables hardware data protection for the boot sectors. This pin cannot be left unconnected.
WP#	INPUT		O	WRITE PROTECT: When low, prevents erasing and programming to all blocks other than boot sector. When WP# is high, it disables hardware data protection for these blocks. This pin cannot be left unconnected.
RES		O	O	RESERVED: These pins must be left unconnected.

Table 1. Pin Descriptions (Continued)

Symbol	Type	Interface		Name and Function
		A/A	FWH	
OE#	INPUT	O		OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	O		WRITE ENABLE: Controls writes to the memory array. Data is latched on the rising edge of WE#.
R/C#	INPUT	O		ROW/COLUMN SELECT: For A/A interface mode, this pin determines whether the address pins are porting to the row address, or to the column address.
A_{10}-A_0	INPUT	O		ADDRESS INPUTS: Inputs for low-order addresses during read and write operations. Addresses are internally latched by R/C# during an erase or program cycle. These addresses share the same pins as the high-order address inputs.
DQ_7-DQ_0	INPUT/ OUTPUT	O		DATA INPUTS/OUTPUTS: Inputs data and commands during write cycles, outputs data during memory array, status register and identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
RY/BY#	OPEN DRAIN OUTPUT	O	O	READY/BUSY#: This output pin is a reflection bit 7 in the status register. This pin is used to determine the erase or program completion. This pin must be pulled-up with an external resistor on board.
V_{CC}	SUPPLY	O	O	DEVICE POWER SUPPLY (3.0V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (refer to DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	O	O	GROUND: Do not float any ground pins.
NC		O	O	NO CONNECT: Lead is not internally connected; it may be driven or floated.

2 Device Operation

2.1 Interface Configuration

The product can operate in two distinct interface modes:

- The FWH interface mode for In-System erasing and programming
- Address/Address Multiplexed (A/A) interface mode for factory erasing and programming

The state of the device's IC pin determines which interface is in use. If the IC pin is set to logic high, the device is in A/A mode; while if the IC pin is set low, the device is in the FWH mode. The IC pin must be configured prior to device operation.

2.2 FWH Mode

The FWH mode uses a 5-signal communication interface, 4-bit address/data bus, FWH_3-FWH_0, and a control line, FWH_4, to control operations of the product. Cycle type operations such as Firmware Memory Read and Firmware Memory Write are defined in Intel Low Pin Count Interface Specification, Rev.1.1. Erase and Program commands sequences are incorporated into the standard FWH memory cycles.

FWH signals are transmitted via the 4-bit Address/Data bus (FWH_3-FWH_0), and follow a particular sequence, depending on whether they are Read or Write operations. The standard FWH memory cycle is defined in Table 2 and Table 3.

2.2.1 FWH_4

The FWH_4 signifies the start of a frame or the termination of a broken frame. Asserting FWH_4 for one or more clock cycle and driving a valid "START" value on FWH_3-FWH_0 will initiate device operation. The device enters standby mode when FWH_4 is high and no internal operation is in progress.

2.2.2 Abort Mechanism

If FWH_4 is driven low for 4 clock cycles during a FWH cycle, the cycle will be terminated and the device will wait for the "ABORT" command. To return the device to the ready mode, the host must drive the FWH_3-FWH_0 with "1111b" ("ABORT" command) while FWH_4 is driven low, and FWH_3-FWH_0 must remain unchanged until FWH_4 goes to V_{IH} (refer to Figure 18). When an abort procedure is performed between the two command write cycles, such as sector/block erase or byte program, the device turns the bus around to the host but the termination of command for the internal operation is not guaranteed. If the system needs to abort after the first command cycle, the host must write "FFH" and check the status register after performing the abort procedure. Status register indicates the termination of internal operation and error conditions. If abort occurs during the internal write cycle, the data may be incorrectly programmed or erased. It is required to wait for the write operation to complete prior to initiation of the abort command. It is recommended to check the write status with status polling (DQ_7) or toggle bit (DQ_6). One other option is to wait for the fixed write time to expire.

2.3 Status Polling DQ_7 (FWH Mode, A/A Mode)

When the product device is in the automatic internal operation (program, erase, etc.), WSM (Write State Machine) status bit DQ_7 (SR.7) will produce a "0". Once the internal operation is completed, DQ_7 will produce a "1". The SR.7 bit can be polled to find the end of the operation. The other status bits (SR.5-0) should not be checked until the WSM completes the operation and the status bit SR.7 is "1". Refer to Table 12 for the status register definition.

2.4 Toggle Bit DQ_6 (FWH Mode, A/A Mode)

During the automatic internal operation (program, erase, etc.), any consecutive attempts to read DQ_6 (SR.6) will produce alternating "0"s and "1"s, i.e., toggling between "0" and "1". When the internal operation is completed, the toggling will stop.

2.5 FWH Memory Cycle Field Definitions

Table 2. FWH Read Cycle Field Definitions

Field	Clocks	FWH_3-FWH_0 Direction	Description
START	1	INPUT	Start of Cycle: "1101b" appears on FWH bus to indicate a FWH memory read cycle.
IDSEL	1	INPUT	Device Select: Indicates which FWH device is selected. The value on FWH_3-FWH_0 is compared to ID strapping values (IDSEL) on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed. Refer to Table 6 for ID strapping values.
MADDR	7	INPUT	Address Phase for Memory Cycle: FWH supports the 28-bit address protocol. It is transferred most significant nibble first. All the values of A_{27}-A_{20} must be set to "1" (refer to Table 6).
MSIZE	1	INPUT	Memory Size: Indicates how many bytes are transferred during Multi Byte Read operation. The product supports four types of multi-byte size. Refer to Table 4 for details. "0000b" = single byte.
TAR	2	INPUT then High Z	Turn-Around: It indicates a turn-around cycle to drive FWH_3-FWH_0 to "1111b" during the first clock and to drive FWH_3-FWH_0 to High Z during the second clock by the host.
Sync	1-3	OUTPUT	Sync: Synchronize to host or peripheral by adding wait states. "0000b" means Ready, "0101b" means Short Wait. The product supports three types of wait states: "no-wait", "1-wait", or "2-waits".
Data	2	OUTPUT	Data Phase: The data byte is transferred least significant nibble first. (DQ_3-DQ_0 on FWH_3-FWH_0 first, DQ_7-DQ_4 on FWH_3-FWH_0 last.)
TAR	2	OUTPUT then High Z	Turn-Around: It indicates a turn-around cycle to drive FWH_3-FWH_0 to "1111b" during the first clock and to drive FWH_3-FWH_0 to High Z during the second clock by the Flash Memory.

Table 3. FWH Write Cycle Field Definitions

Field	Clocks	FWH_3-FWH_0 Direction	Description
START	1	INPUT	Start of Cycle: "1110b" appears on FWH bus to indicate a FWH memory write cycle.
IDSEL	1	INPUT	Device Select: Indicates which FWH device is selected. The value on FWH_3-FWH_0 is compared to ID strapping values (IDSEL) on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed. Refer to Table 6 for ID strapping values.
MADDR	7	INPUT	Address Phase for Memory Cycle: FWH supports the 28-bit address protocol. It is transferred most significant nibble first. All the values of A_{27}-A_{20} must be set to "1" (refer to Table 6).
MSIZE	1	INPUT	Memory Size: The product only supports single-byte program. (Always "0000b")
Data	2	INPUT	Data Phase: The data byte is transferred least significant nibble first. (DQ_3-DQ_0 on FWH_3-FWH_0 first, DQ_7-DQ_4 on FWH_3-FWH_0 last.)
TAR	2	INPUT then High Z	Turn-Around: It indicates a turn-around cycle to drive FWH_3-FWH_0 to "1111b" during the first clock and to drive FWH_3-FWH_0 to High Z during the second clock by the last components driving FWH_3-FWH_0.
Sync	1	OUTPUT	Sync: The product only supports "0000b" Ready sync.
TAR	2	OUTPUT then High Z	Turn-Around: It indicates a turn-around cycle to drive FWH_3-FWH_0 to "1111b" during the first clock and to drive FWH_3-FWH_0 to High Z during the second clock by the Flash Memory.

2.6 Multi Byte Read (FWH Mode)

The product provides Multi Byte Read operation in FWH mode. Multi Byte Read mode enables two or more byte of sequential read at one operation cycle. This increases data transfer rate compared with normal memory read operation. The transfer multi-byte size can be selected from four types.

Table 4. FWH Multi Byte Read Cycle Field Definitions

<table>
<tr><th>Field</th><th>Clocks</th><th>FWH_3-FWH_0 Direction</th><th>Description</th></tr>
<tr><td>START</td><td>1</td><td>INPUT</td><td>Start of Cycle: "1101b" appears on FWH bus to indicate the start of cycle.</td></tr>
<tr><td>IDSEL</td><td>1</td><td>INPUT</td><td>Device Select: Indicates which FWH device is selected: "0000b" to "1111b".</td></tr>
<tr><td>MADDR</td><td>7</td><td>INPUT</td><td>Address: Start address of Multi Byte Read: A_{27}-A_0.</td></tr>
<tr><td>MSIZE</td><td>1</td><td>INPUT</td><td>Transfer Multi-Byte Size:
"0000b" = 1 byte
<table>
<tr><th>FWH_3-FWH_0</th><th>Transfer Byte Size</th></tr>
<tr><td>1000</td><td>2 byte</td></tr>
<tr><td>1001</td><td>8 byte</td></tr>
<tr><td>1010</td><td>32 byte</td></tr>
<tr><td>1011</td><td>128 byte</td></tr>
</table></td></tr>
<tr><td>TAR</td><td>2</td><td>INPUT then High Z</td><td>Turn-Around: "1111b" and High Z</td></tr>
<tr><td>Sync 1</td><td>N+1</td><td>OUTPUT</td><td>Sync: "0101b" = Short Wait (N: the number of Short Wait)
"0000b" = Ready</td></tr>
<tr><td>Data 1</td><td>2</td><td>OUTPUT</td><td>Data Phase: First byte; DQ_3-DQ_0 on FWH_3-FWH_0 (1st. cycle)
DQ_7-DQ_4 on FWH_3-FWH_0 (2nd. cycle)</td></tr>
<tr><td>Sync M</td><td>(N+1) × M</td><td>OUTPUT</td><td>Sync: "0101b" = Short Wait (N: the number of Short Wait)
"0000b" = Ready (M: the number of Multi Byte)</td></tr>
<tr><td>Data M</td><td>2 × M</td><td>OUTPUT</td><td>Data Phase: Multi byte; DQ_3-DQ_0 on FWH_3-FWH_0 (1st. cycle)
DQ_7-DQ_4 on FWH_3-FWH_0 (2nd. cycle)</td></tr>
<tr><td>TAR</td><td>2</td><td>OUTPUT then High Z</td><td>Turn-Around: "1111b" and High Z</td></tr>
</table>

Table 5. FWH Multi Byte Read Bandwidth [f(CLK)=33MHz]

128-Byte Multi Byte Read	Clocks		Unit
START	1		
IDSEL	1		
MADDR	7		
MSIZE	1		
TAR	2		
Sync (no-wait)	1	× 128	
Data	2		
TAR	2		
Total Clocks	398		
Transfer Time	12		µs
Bandwidth	10.69		MByte/s

128-Byte Normal Read	Clocks		Unit
START	1	× 128	
IDSEL	1		
MADDR	7		
MSIZE	1		
TAR	2		
Sync (no-wait)	1		
Data	2		
TAR	2		
Total Clocks	17 × 128		
Transfer Time	65		µs
Bandwidth	1.96		MByte/s

2.7 Multiple Device Selection (FWH Mode)

Multiple FWH Flash devices may be strapped to increase memory densities in a system. FWH protocol of the product supports up to 16 FWH Flash devices.

The four ID pins, ID_3-ID_0, allow up to 16 devices to be attached to the same bus by using different ID strapping in a system. If the product is used as a boot device, ID_3-ID_0 must be strapped as "0000", all subsequent devices should use a sequential up-count strapping (i.e., "0000", "0100", "1000", "1100", etc.).

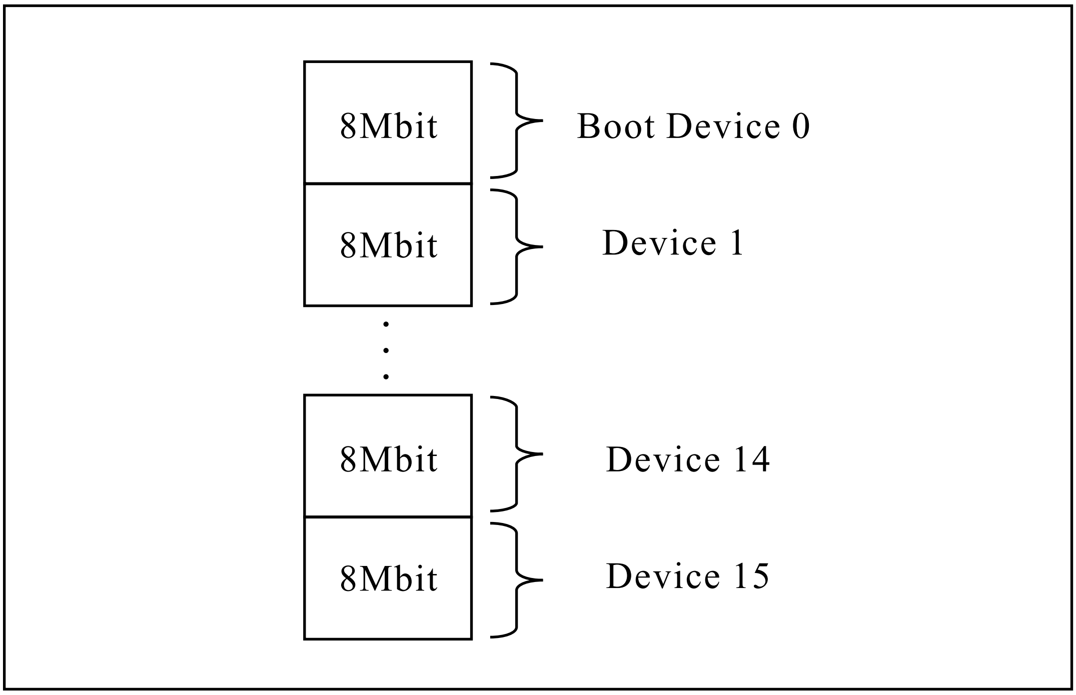


Figure 2. Multiple FWH Device Mapping

Table 6. ID Strapping Values (FWH Mode)

<table>
<tr><th>Device No.</th><th>ID_3-ID_0 = IDSEL</th><th>A_{27}-A_{23}</th><th>A_{22}</th><th>A_{21}-A_{20}</th></tr>
<tr><td>0 (Boot device)</td><td>0000</td><td rowspan="12">11111</td><td rowspan="12">Read:
1 = Memory Read
0 = Register Read

Write:
0 or 1 = Memory Write</td><td rowspan="12">11</td></tr>
<tr><td>1</td><td>0001</td></tr>
<tr><td>2</td><td>0010</td></tr>
<tr><td>3</td><td>0011</td></tr>
<tr><td>4</td><td>0100</td></tr>
<tr><td>5</td><td>0101</td></tr>
<tr><td>6</td><td>0110</td></tr>
<tr><td>7</td><td>0111</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>14</td><td>1110</td></tr>
<tr><td>15</td><td>1111</td></tr>
</table>

2.8 General Purpose Inputs (GPI) Register (FWH Mode)

The GPI_REG (General Purpose Inputs Register) reads the status of the $FGPI_4$-$FGPI_0$ pins on the product. Since this is a pass-through register, there is no default value, only the state of the pins at power-up. The pins must have stable data from before the start of the cycle that reads the GPI_REG until after the cycle is complete. These pins must not be left to float and they should be driven V_{IL} or V_{IH}.

Refer to Table 7 for the GPI_REG bits and function. If the address shown in Table 8 is input, GPI_REG can be read also on read identifier codes mode, read status register mode or read array mode.

Table 7. General Purpose Input Register

Bit	Function
7:5	Reserved for future implementation.
4	$FGPI_4$: Reads status of general-purpose input pin (Pin 7)
3	$FGPI_3$: Reads status of general-purpose input pin (Pin 15)
2	$FGPI_2$: Reads status of general-purpose input pin (Pin 16)
1	$FGPI_1$: Reads status of general-purpose input pin (Pin 17)
0	$FGPI_0$: Reads status of general-purpose input pin (Pin 18)

2.9 Product Identifier Codes (FWH Mode, A/A Mode)

The product identifier codes identify the device as the product and manufacturer as SHARP.

• In FWH mode:

The Read Identifier Codes command is unnecessary and only an address shown in Table 8 is required. However, A_{22} must be "0" in this operation. The operation by the command is also possible if the Read Identifier Codes command is written. Any command is acceptable not only when A_{22}="1" but also when A_{22}="0".

• In A/A mode:

The Read Identifier Codes command is necessary. Refer to Table 11 for the command definitions.

2.10 Lock Registers (FWH Mode, A/A Mode)

The product offers double write protection. The boot lock provides hardware write protection for each 8-Kbyte boot sector. Furthermore, the whole block lock provides software write protection for all sectors and blocks. The write protection status is controlled by each lock bit. Refer to "2.11 Write Protection" for details. The protection status can be checked through the lock registers.

Table 8. FWH Flash Registers Configuration Map (1), (3), (5)

Device Address		Register Name	Protected Address Range $[A_{19}-A_0]$	Default Value	Type	Notes
A_{22} (2)	$[A_{19}-A_0]$					
0 (Register Access)	XX002H	Whole Block Lock Register	FFFFFH - 00000H	$DQ_1 = 1$	RO	4
	FE002H	Block Lock Register (Sector 7)	FFFFFH - FE000H	$DQ_0 = 0$	RO	4
	FC002H	Block Lock Register (Sector 6)	FDFFFH - FC000H	$DQ_0 = 0$	RO	4
	FA002H	Block Lock Register (Sector 5)	FBFFFH - FA000H	$DQ_0 = 0$	RO	4
	F8002H	Block Lock Register (Sector 4)	F9FFFH - F8000H	$DQ_0 = 0$	RO	4
	F6002H	Block Lock Register (Sector 3)	F7FFFH - F6000H	$DQ_0 = 0$	RO	4
	F4002H	Block Lock Register (Sector 2)	F5FFFH - F4000H	$DQ_0 = 0$	RO	4
	F2002H	Block Lock Register (Sector 1)	F3FFFH - F2000H	$DQ_0 = 0$	RO	4
	F0002H	Block Lock Register (Sector 0)	F1FFFH - F0000H	$DQ_0 = 0$	RO	4
	C0100H	FWH General Purpose Input Register	N/A	N/A	RO	
	00001H	Device Code Register	N/A	CFH	RO	
	00000H	Manufacturer Code Register	N/A	B0H	RO	

NOTES:
1. $A_{27}-A_{20}$ are not used in A/A mode.
2. A_{22} must be "0" when the registers are read in FWH mode.
3. $A_{27}-A_{23}$ and $A_{21}-A_{20}$ must be "1" in FWH mode.
4. DQ_7-DQ_2 are reserved for future implementation.
5. The registers shown above must not be read while the WSM is busy.

2.11 Write Protection

2.11.1 TBL# and WP# Hardware Write Protection (FWH Mode)

The top boot lock (TBL#) and write protect (WP#) pins are provided for hardware write protection of the memory area in the product. TBL# pin is used to write protection of 8 boot sectors (8Kbytes) at the highest memory address range for the product. WP# pin is used for the remaining blocks in the flash memory.

An active low signal at the TBL# pin prevents erase and program operations of the boot sectors. TBL# protection is effective only to the sector to which the boot lock bit is set. When TBL# pin is held high, the write protection of the boot sectors is disabled. The WP# pin serves the same function for the remaining blocks of the memory array. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting an erase or program operation. A logic level change occurring at the TBL# or WP# pin during an erase or program operation could cause unpredictable results.

2.11.2 Whole Block Lock Software Write Protection (FWH Mode, A/A Mode)

The whole block lock is provided for software write protection of the memory area in the product. Whole block lock protects all sectors and blocks in the device by lock bit. The lock bit is set to locked state in an initial state after power-up or reset operation. The lock bit must be cleared to unlocked state before starting erase or program operation. The lock bit is cleared by clear whole block lock bit operation. After erase or program operation is finished, the memory array can be protected by set whole block lock bit operation.

Table 9. Write Protection Alternatives

Operation	Whole Block Lock Bit [1]	TBL#	Boot Lock Bit [1]	WP#	Effect
Sector Erase or Block Erase or Full Chip Erase or Byte Program	1	X	X	X	All sectors and blocks are Locked.
	0	V_{IL}	1	X	Boot sector is Locked.
		V_{IL}	0	X	Boot sector is Unlocked.
		V_{IH}	X	X	All boot sectors are Unlocked
		V_{IH}	X	V_{IL}	The remaining blocks other than boot sectors are Locked
		V_{IH}	X	V_{IH}	All sectors and blocks are Unlocked

NOTES:
1. Lock Bit : "1" = Locked State, "0" = Unlocked State

2.12 Memory Map

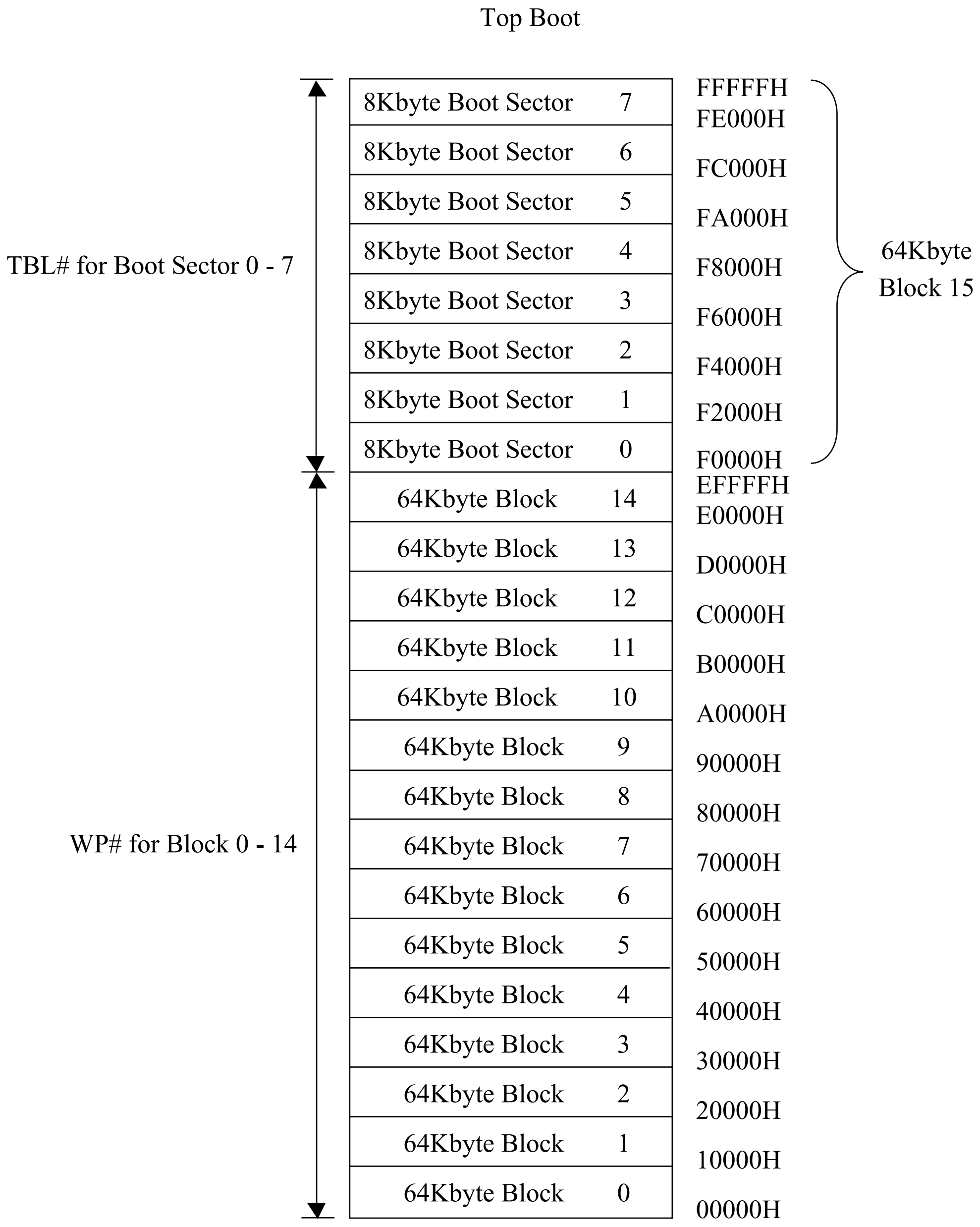


Figure 3. Memory Map

2.13 A/A Mode

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#.

During the software command sequence, the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Table 10. Operation Modes Selection (1)

Mode	Notes	RST#	OE#	WE#	Address	DQ (2)
Read Array	6	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Output Disable		V_{IH}	V_{IH}	V_{IH}	X	High Z
Standby		V_{IH}	V_{IH}	V_{IH}	X	High Z
Reset	3	V_{IL}	X	X	X	High Z
Read Identifier Codes	6	V_{IH}	V_{IL}	V_{IH}	Refer to Table 8	Refer to Table 8
Read Status Register	6	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Write	4, 5, 6	V_{IH}	V_{IH}	V_{IL}	A_{IN}	D_{IN}

NOTES:
1. X can be V_{IL} or V_{IH} for control pins and addresses.
2. DQ refers to DQ_7-DQ_0.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits are reliably executed when V_{CC}=3.0V-3.6V.
5. Refer to Table 11 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.

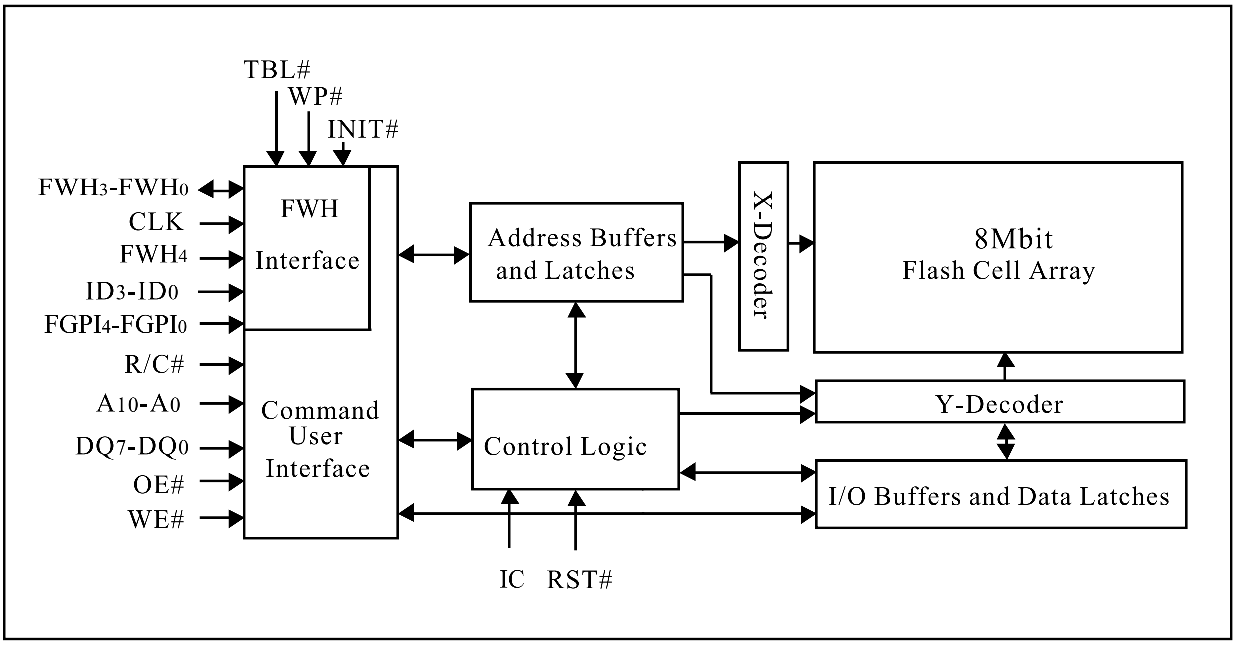


Figure 4. Block Diagram

2.14 Command Definitions

Table 11. Command Definitions (12)

Command	Interface		Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
	A/A	FWH			Oper(1)	Addr(2)	Data	Oper(1)	Addr(2)	Data(3)
Read Array	O	O	1	4	Write	X	FFH			
Read Identifier Codes	O	O	≥ 2	5	Write	X	90H	Read	IA	ID
Read Status Register	O	O	2		Write	X	70H	Read	X	SRD
Clear Status Register	O	O	1	4	Write	X	50H			
Sector/Block Erase	O	O	2	6,7	Write	BA	20H	Write	BA	D0H
Full Chip Erase	O		2	6,7,8	Write	X	30H	Write	X	D0H
Byte Program	O	O	2	6,7,9	Write	X	40H or 10H	Write	WA	WD
Set Whole Block Lock Bit	O	O	2		Write	X	60H	Write	X	BBH
Clear Whole Block Lock Bit	O	O	2	7	Write	X	60H	Write	X	DBH
Set Boot Lock Bit	O	O	2	10	Write	X	60H	Write	SA	01H
Clear Boot Lock Bits	O	O	2	11	Write	X	60H	Write	SA	D0H

NOTES:
1. Bus operations are defined in Table 10.
2. Any command is acceptable not only when A_{22}="1" but also when A_{22}="0" in FWH mode.
   X=Any valid address within the device.
   IA=Identifier codes address (Refer to Table 8).
   BA=Address within the sector/block for sector/block erase.
   WA=Address of memory location for program.
   SA=Address within the boot sector for set boot lock bit.
3. ID=Data to be read from identifier codes. (Refer to Table 8).
   SRD=Data to be read from status register. Refer to Table 12 for a description of the status register bits.
   WD=Data to be programmed at location WA.
4. The device returns to the read array mode even after Clear Status Register command or reset operation by RST#/INIT#.
5. Following the Read Identifier Codes command, read operations access manufacturer code, device code and block lock configuration code (Refer to Table 8). The identifier codes must not be read while the WSM is busy.
6. Sector/block erase, full chip erase and byte program operations cannot be executed to boot sector when TBL# goes to V_{IL}. Sector/block erase, full chip erase and byte program operations cannot be executed to blocks other than boot sector when WP# goes to V_{IL}.
7. Whole block lock bit must be cleared when executing sector/block erase, full chip erase and byte program operations. Sector/block erase, full chip erase and byte program operations cannot be executed if whole block lock bit is set.
8. Supported in A/A Mode only. Any boot sector which is locked by boot lock bit is protected from alteration. Boot lock bit should be cleared before performing an erase operation.
9. Either 40H or 10H are recognized as the program first bus cycle command.
10. Lock bit can be set to each sector within the boot block (block 15). Since this lock bit is non-volatility, it holds the lock state even after power-off or reset.
11. All boot lock bits of each sector are cleared at a time.
    SA=Address within the boot sector (F0000H-FFFFFH).
12. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

2.15 Status Register Definition

Table 12. Status Register Definition

WSMS	TB	ECLS	PSLS	PVEVS	R	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check SR.7 or SR.6 or RY/BY# to determine sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit or clear boot lock bits completion. SR.5, SR.4, SR.3 and SR.1 are invalid while SR.7="0".
SR.6 = TOGGLE BIT (TB) Toggling between "0" and "1" during the erase or program operation.	
SR.5 = SECTOR/BLOCK ERASE, FULL CHIP ERASE AND CLEAR BOOT LOCK BITS STATUS (ECLS) 1 = Error in Sector/Block Erase, Full Chip Erase or Clear Boot Lock Bits 0 = Successful Sector/Block Erase, Full Chip Erase or Clear Boot Lock Bits	If both SR.5 and SR.4 are "1"s after a sector/block erase, full chip erase, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits attempt, an improper command sequence was entered.
SR.4 = BYTE PROGRAM AND SET BOOT LOCK BIT STATUS (PSLS) 1 = Error in Byte Program or Set Boot Lock Bit 0 = Successful Byte Program or Set Boot Lock Bit	SR.3 indicates the program or erase voltage conditions. The program or erase voltage is the internal voltage which is used for the program or erase operation in the flash memory. SR.3 does not provide a continuous indication of the program or erase voltage level. The WSM interrogates and indicates the program or erase voltage level only after Sector/Block Erase, Full Chip Erase, Byte Program, Set Boot Lock Bit and Clear Boot Lock Bits command sequences.
SR.3 = PROGRAM VOLTAGE OR ERASE VOLTAGE STATUS (PVEVS) 1 = Invalid Program or Erase Voltage Detect, Operation Abort 0 = Program or Erase Voltage OK	
SR.2 = RESERVED FOR FUTURE ENHANCEMENTS (R)	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block by TBL#, WP# or Block Lock Bit, Operation Abort 0 = Unlocked	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates TBL#, WP# or block lock bit only after Sector/Block Erase, Full Chip Erase or Byte Program command sequences. It informs the system, depending on the attempted operation, if the block is locked.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.2 and SR.0 are reserved for future use and should be masked out when polling the status register.

3 Electrical Specifications

3.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...... 0°C to +85°C (1)

Storage Temperature

During under Bias............................... -10°C to +85°C

During non Bias................................ -65°C to +125°C

Voltage On Any Pin

(except V_{CC})............................ -0.5V to V_{CC}+0.5V (2)

V_{CC} Supply Voltage .... -0.2V to +3.9V (2)

Output Short Circuit Current........................... 100mA (3)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for commercial temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} pin. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

3.2 Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Operating Temperature		0	+25	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage	1	3.0	3.3	3.6	V	
	Sector/Block Erase Cycling		100,000			Cycles	

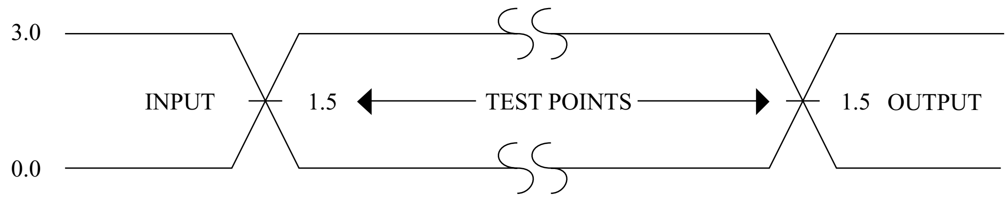
NOTES:
1. Refer to DC Characteristics tables for voltage range-specific specification.

3.2.1 Capacitance (1) (T_A=+25°C, f=1MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance		7	10	pF	V_{IN}=0.0V
$C_{I/O}$	Input / Output Capacitance		9	12	pF	$V_{I/O}$=0.0V

NOTE:
1. Sampled, not 100% tested.

3.2.2 AC Input/Output Test Conditions



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0".
Input timing begins and output timing ends at 1.5V. Input rise and fall times (10% to 90%) < 5ns.

Figure 5. Transient Input/Output Reference Waveform for V_{CC}=3.0V-3.6V

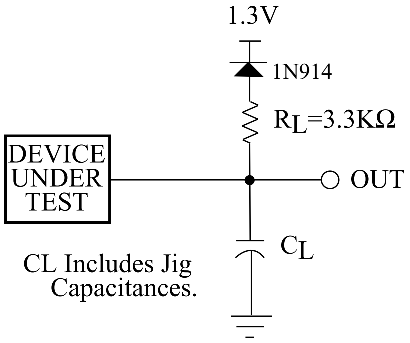


Figure 6. Transient Equivalent Testing Load Circuit

Table 13. Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=3.0V-3.6V	30

3.2.3 DC Characteristics

V_{CC}=3.0V-3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current	1	-1		+1	µA	$V_{CC}=V_{CC}$Max., $V_{IN}/V_{OUT}=V_{CC}$ or GND
I_{LID}	Input Load Current for IC, ID_3-ID_0 pins	1	-200		+200	µA	
I_{LO}	Output Leakage Current	1	-1		+1	µA	
I_{CCS1}	V_{CC} Standby Current (FWH Interface)	1, 2, 5		5	15	µA	CMOS Inputs, $V_{CC}=V_{CC}$Max., f(CLK)=33MHz $FWH_4=V_{IH}$, RST#=V_{CC}±0.2V
I_{CCRY}	V_{CC} Ready Mode Current (FWH Interface)	1, 2, 5		5	8	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., f(CLK)=33MHz $FWH_4=V_{IL}$, RST#=V_{CC}±0.2V
I_{CCS2}	V_{CC} Standby Current (A/A Interface)	1, 2, 5		5	8	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., RST#=V_{CC}±0.2V, R/C#=OE#=WE#=V_{IH}
I_{CCD}	V_{CC} Reset Current	1		5	15	µA	RST#=GND±0.2V, I_{OUT} (RY/BY#)=0mA
I_{CCR1}	V_{CC} Read Current (FWH Interface)	1, 2			15	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., $FWH_4=V_{IL}$, f(CLK)=33MHz, I_{OUT}=0mA
I_{CCR2}	V_{CC} Read Current (A/A Interface)	1, 2			15	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max., f=4MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Byte Program, Set Boot Lock Bit Current	1, 2, 4			25	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max.
I_{CCE}	V_{CC} Sector/Block Erase, Full Chip Erase, Clear Boot Lock Bits Current	1, 2, 4			25	mA	CMOS Inputs, $V_{CC}=V_{CC}$Max.

DC Characteristics (Continued)

V_{CC}=3.0V-3.6V

Symbol	Parameter	Notes	Min.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	4	0.5× V_{CC}	V_{CC} + 0.5	V	V_{CC}=V_{CC}Max.,
V_{IL}	Input Low Voltage	4	-0.5	0.3× V_{CC}	V	V_{CC}=V_{CC}Min.,
V_{OH}	Output High Voltage	4	0.9× V_{CC}		V	V_{CC}=V_{CC}Min., I_{OH}=-0.5mA
V_{OL}	Output Low Voltage	4, 5		0.1× V_{CC}	V	V_{CC}=V_{CC}Min., I_{OL}=1.5mA
V_{LKO}	V_{CC} Lockout Voltage	3	2.0		V	

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC}=3.3V and T_A=+25°C unless V_{CC} is specified.
2. CMOS inputs are either V_{CC}±0.2V or GND±0.2V.
3. Sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits operations are inhibited when V_{CC}≤V_{LKO}. These operations are not guaranteed outside the specified voltage (V_{CC}=3.0V-3.6V).
4. Sampled, not 100% tested.
5. Includes RY/BY#.

3.2.4 AC Characteristics (FWH Mode) (1)

AC Characteristics (FWH Mode)

V_{CC}=3.0V~3.6V, T_A=0°C~+85°C

Symbol	Parameter	Notes	Min.	Typ.(2)	Max.	Unit
t_{CYC}	Clock Cycle Time		30			ns
t_{HIGH}	CLK High Time		11			ns
t_{LOW}	CLK Low Time		11			ns
	CLK Slew Rate (peak-to-peak)		1		4	V/ns
t_{SU}	Data Set-up Time to Clock Rising		9			ns
t_{DH}	Data Hold Time from Clock Rising		0			ns
t_{FSU}	FWH_4 Set-up Time to Clock Rising		18			ns
t_{FDH}	FWH_4 Hold Time from Clock Rising		2			ns
t_{VAL}	Clock Rising to Data Valid		2		15	ns
t_{ON}	Clock Rising to Output in Low Z	3	2			ns
t_{OFF}	Clock Rising to Output in High Z	3			28	ns
t_{WQV1}	Byte Program Time	3, 4		25	200	µs
t_{WQV2}	Sector Erase Time	3, 4		0.6	5	s
t_{WQV3}	Block Erase Time	3, 4		1.2	6	s
t_{WQV4}	Full Chip Erase Time	3, 4		40	200	s
t_{SWBL}	Set Whole Block Lock Bit Time	3, 4		5	8	µs
t_{CWBL}	Clear Whole Block Lock Bit Time	3, 4		5	8	µs
t_{STBL}	Set Boot Lock Bit Time	3, 4		35	200	µs
t_{CTBL}	Clear Boot Lock Bits Time	3, 4		0.4	1	s

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Typical values measured at V_{CC}=3.3V and T_A=+25°C. Assumes TBL#, WP# and corresponding lock bits are not set. Subject to change based on device characterization.
3. Sampled, not 100% tested.
4. Excludes external system-level overhead.

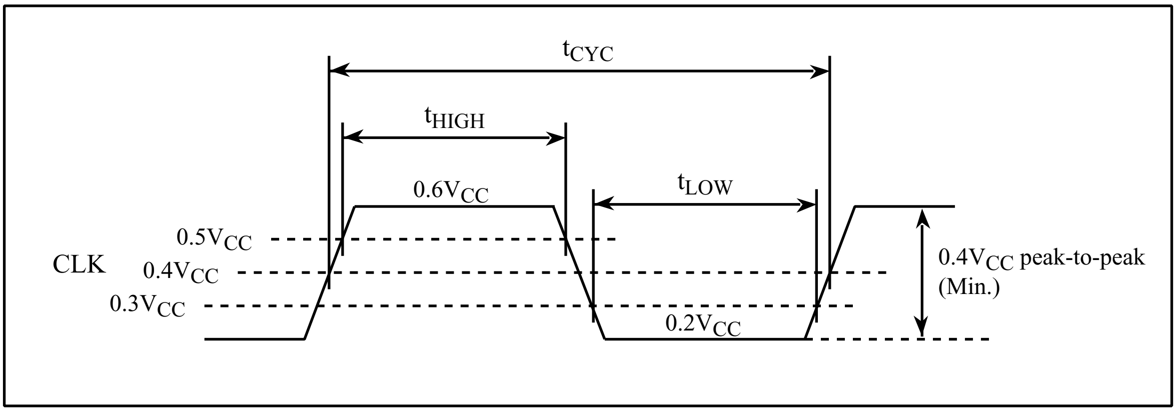


Figure 7. CLK Waveform

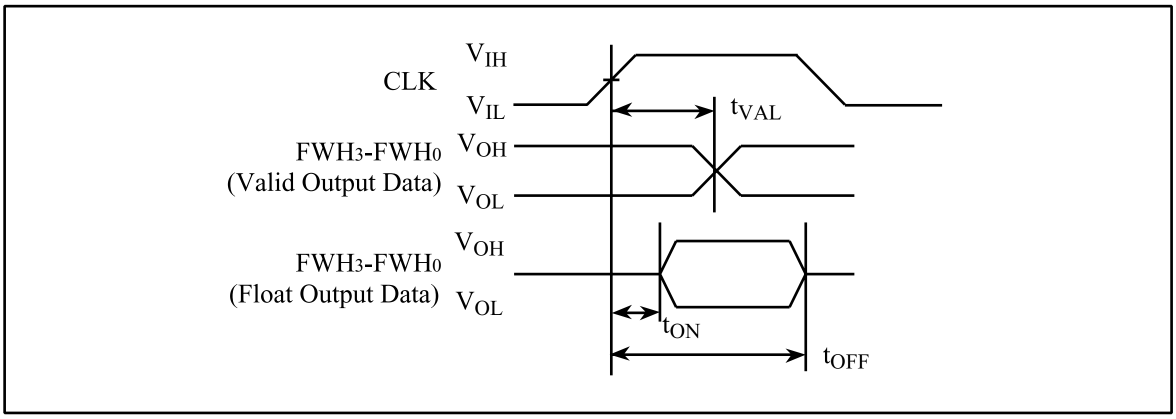


Figure 8. Output Timing Parameters

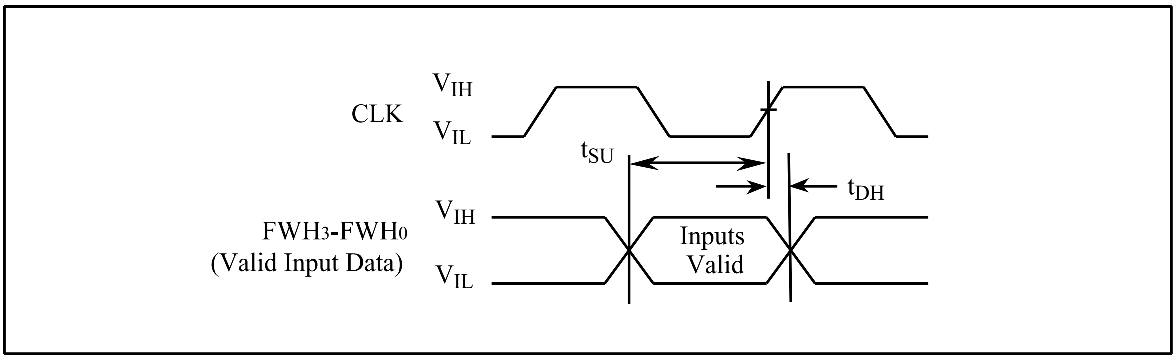
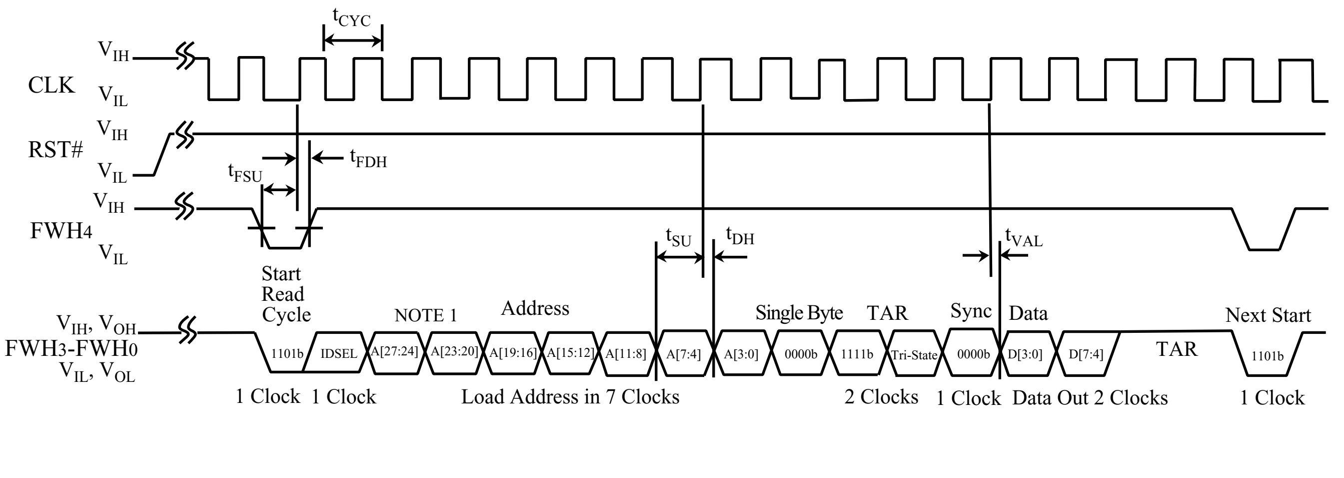
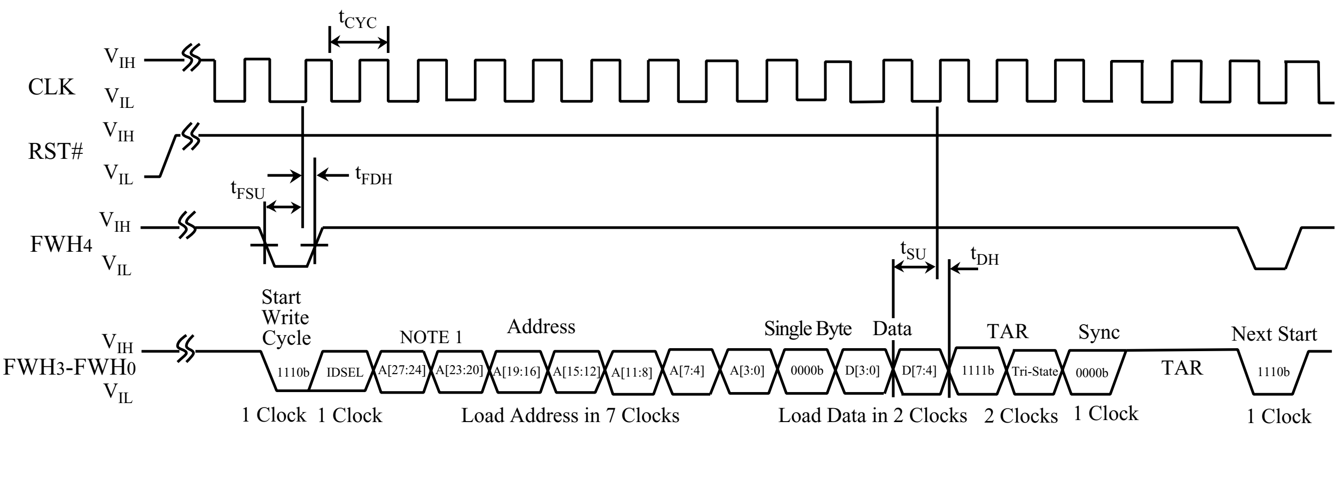


Figure 9. Input Timing Parameters



NOTE 1. All the values of A[27:20] must be "1".

Figure 10. Read Cycle Timing Diagram (FWH Mode)



NOTE 1. All the values of A[27:20] must be "1".

Figure 11. Write Cycle Timing Diagram (FWH Mode)

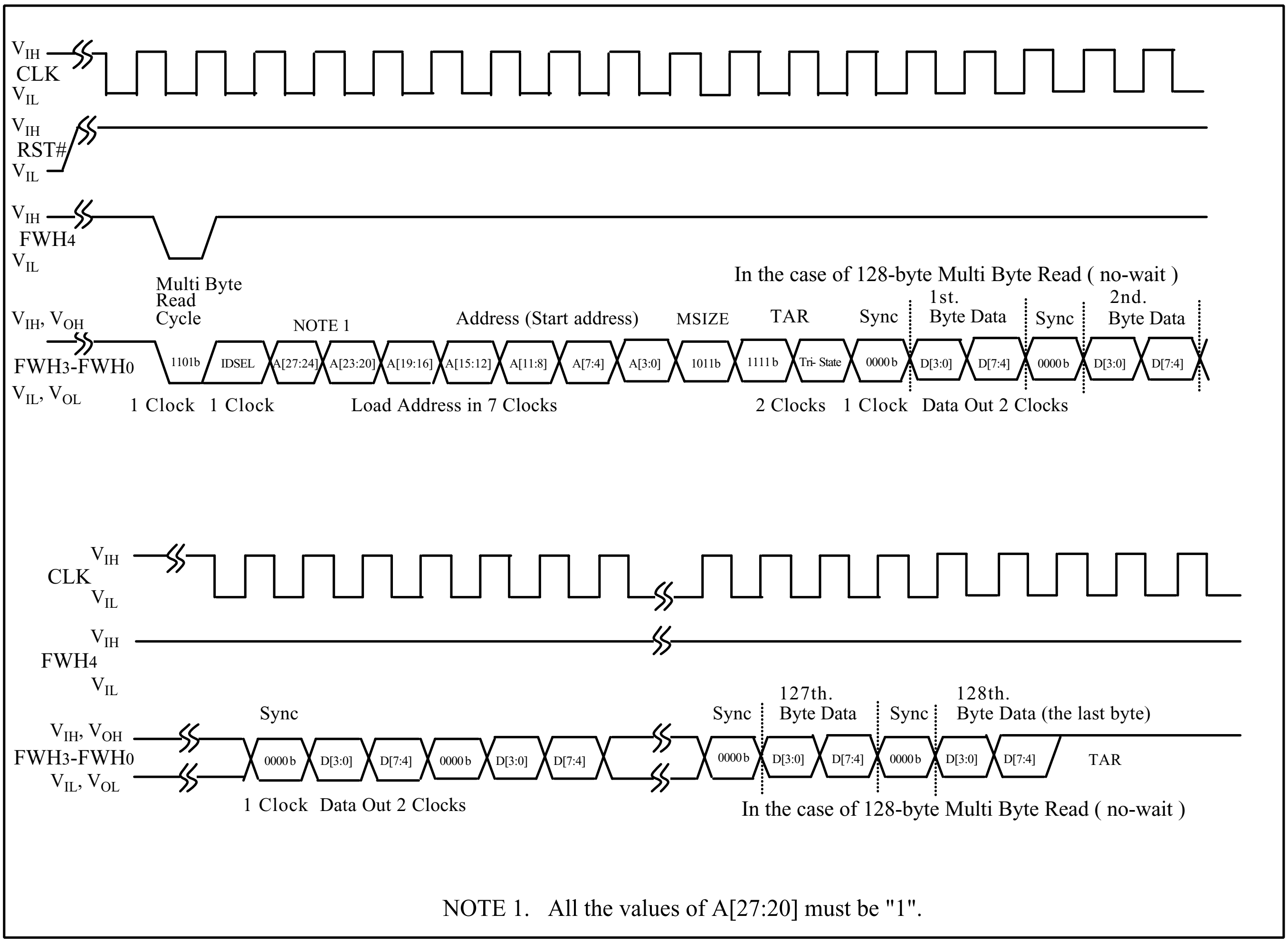


Figure 12. Multi Byte Read Cycle Timing Diagram (FWH Mode)

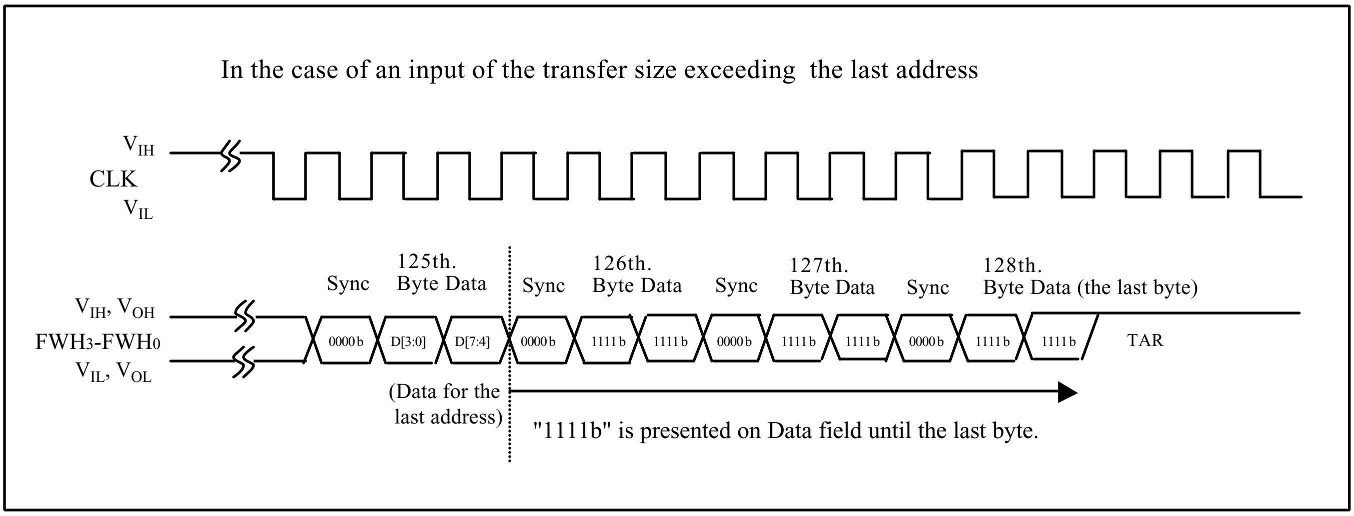
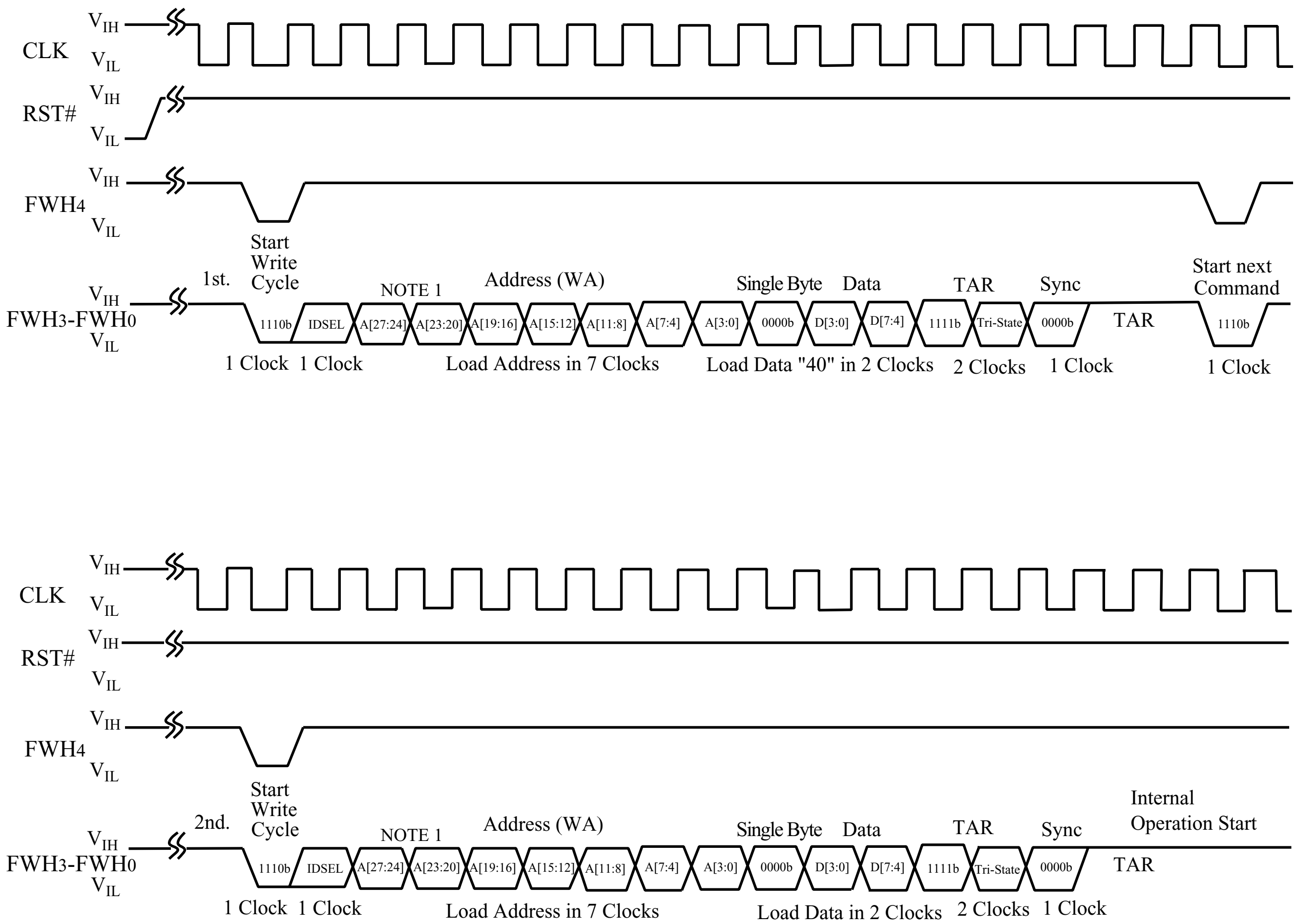
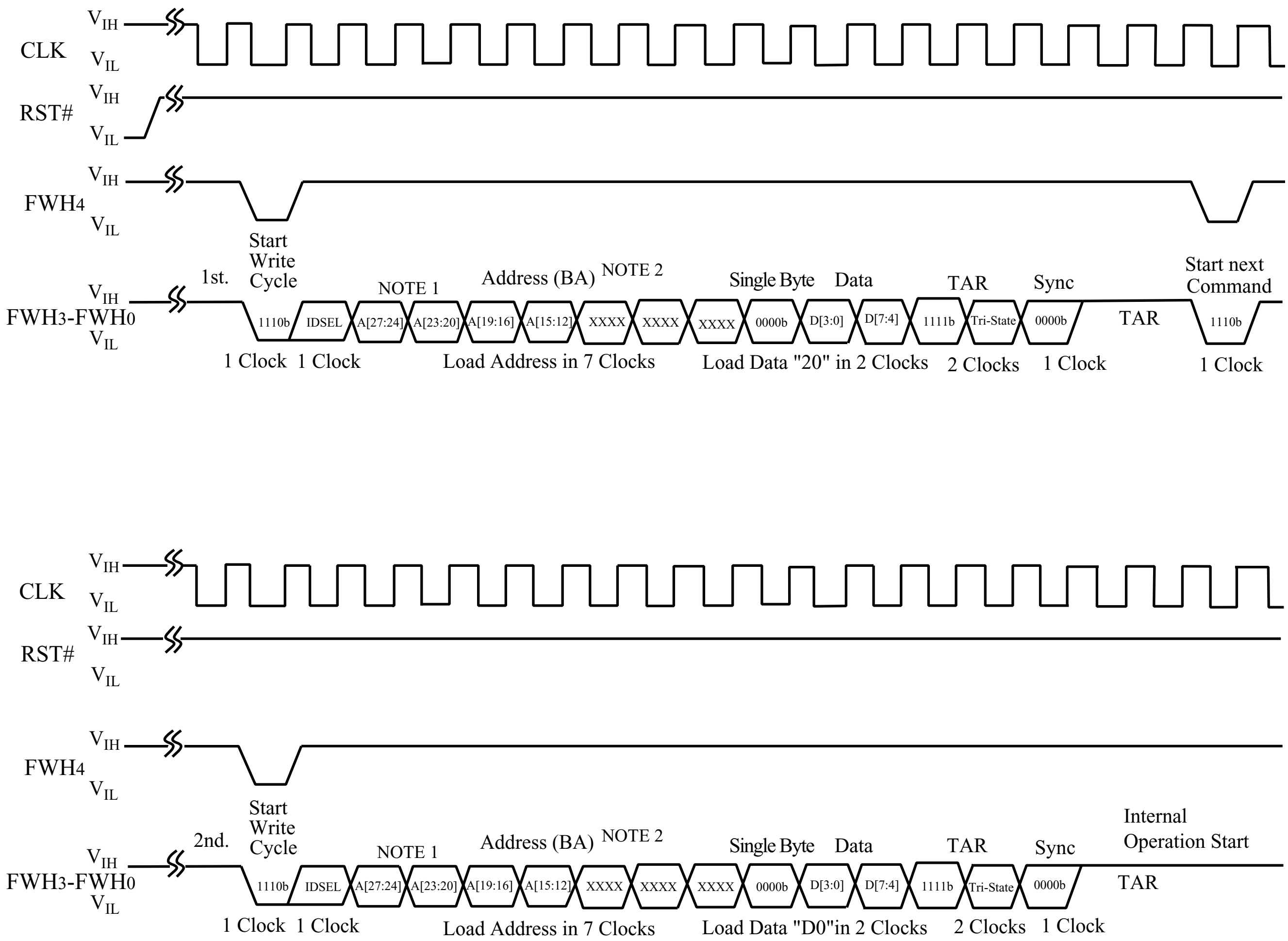


Figure 13. Multi Byte Read Exceeding the Last Address (FWH Mode)



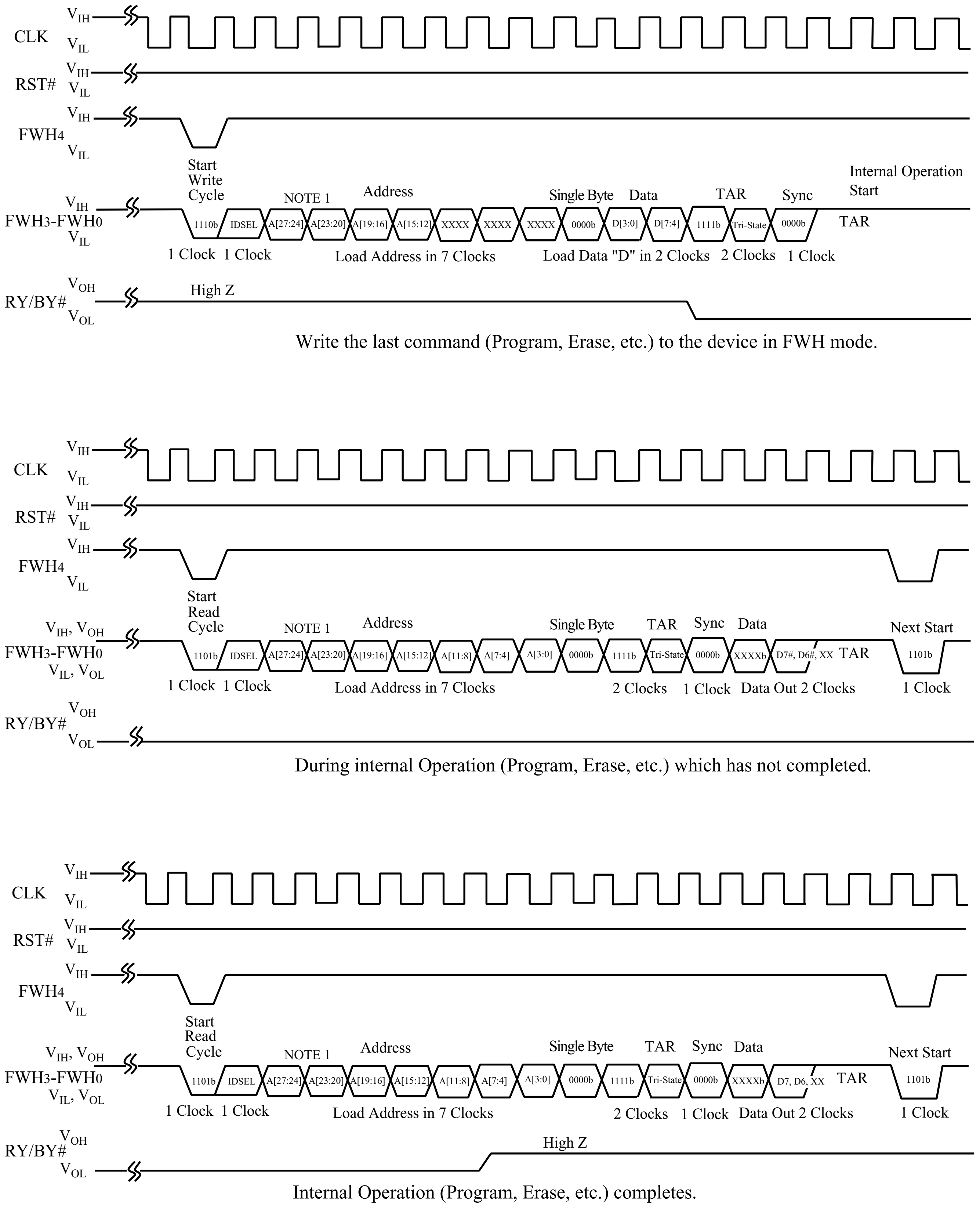
NOTE 1. All the values of A[27:20] must be "1".

Figure 14. Byte Program Cycle Timing Diagram (FWH Mode)



NOTE 1. All the values of A[27:20] must be "1".
NOTE 2. BA = Sector / Block Address : A_{11}-A_0 may be "0" or "1".

Figure 15. Sector/Block Erase Cycle Timing Diagram (FWH Mode)



NOTE 1. All the values of A[27:20] must be "1".

Figure 16. Status Polling, Toggle Bit Timing Diagram (FWH Mode)

3.2.5 Reset and Abort Operations (FWH Mode)

Reset and Abort Characteristics (FWH Mode)

V_{CC}=3.0V~3.6V, T_A=0°C~+85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PRSTH}	V_{CC} 3.0V stable to RST#/INIT# High	2	100		ns
t_{PRSTL}	V_{CC} 3.0V stable to RST#/INIT# Low	2	1		ms
t_{KRST}	Clock stable to RST#/INIT# Low	2	100		µs
t_{RSTP}	RST#/INIT# Pulse Width Low	1, 2	100		ns
	RST#/INIT# Slew Rate	2	50		mV/ns
t_{RSTF}	RST#/INIT# Low to Output in High Z	2		48	ns
t_{RSTL}	RST#/INIT# High to FWH_4 Low	2, 3	1		µs
t_{ABTL}	Abort Command to FWH_4 Low	2	60		ns
t_{RSTE}	RST#/INIT# Low to Reset during internal operation	2, 4		30	µs

NOTES:
1. The device may reset if t_{RSTP} < 100ns, but this is not guaranteed.
2. Sampled, not 100% tested.
3. There will be a latency of t_{RSTE} if a reset/abort procedure is performed during an internal operation.
4. If RST#/INIT# asserted while a sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits operations are not executing, the reset will complete within 100ns.

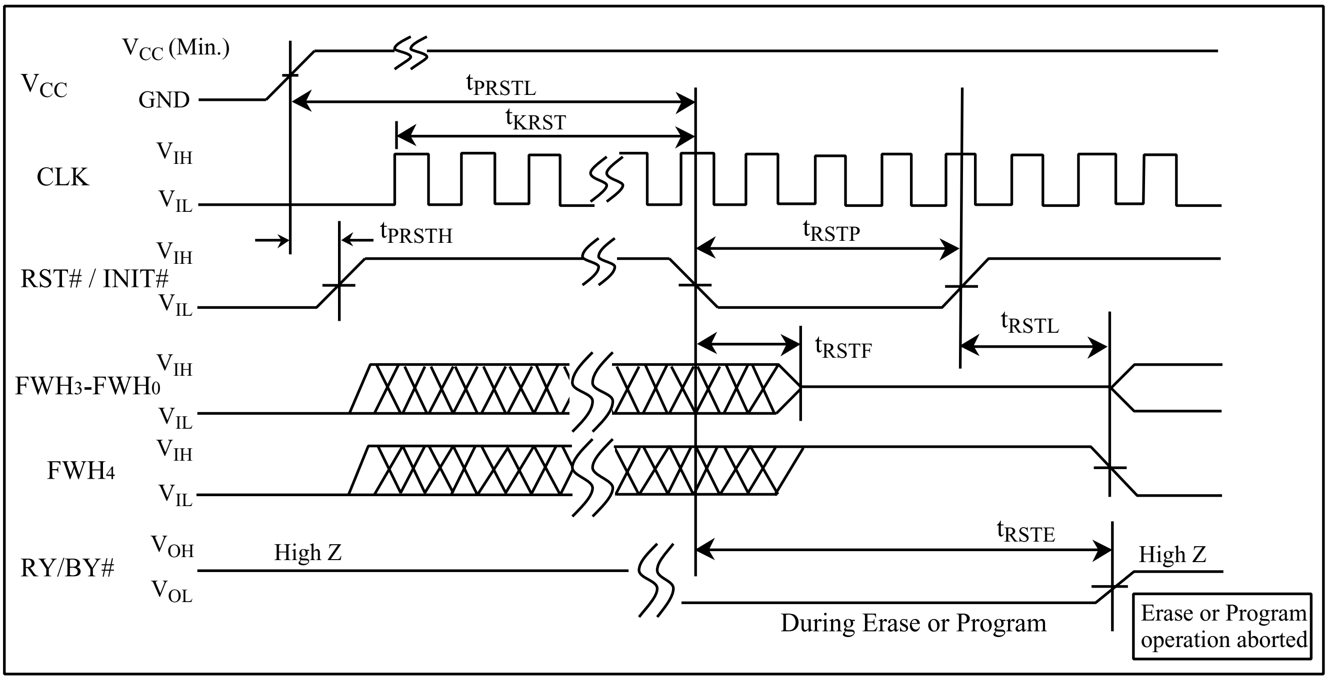


Figure 17. Reset Operation by RST#/INIT# Timing Diagram (FWH Mode)

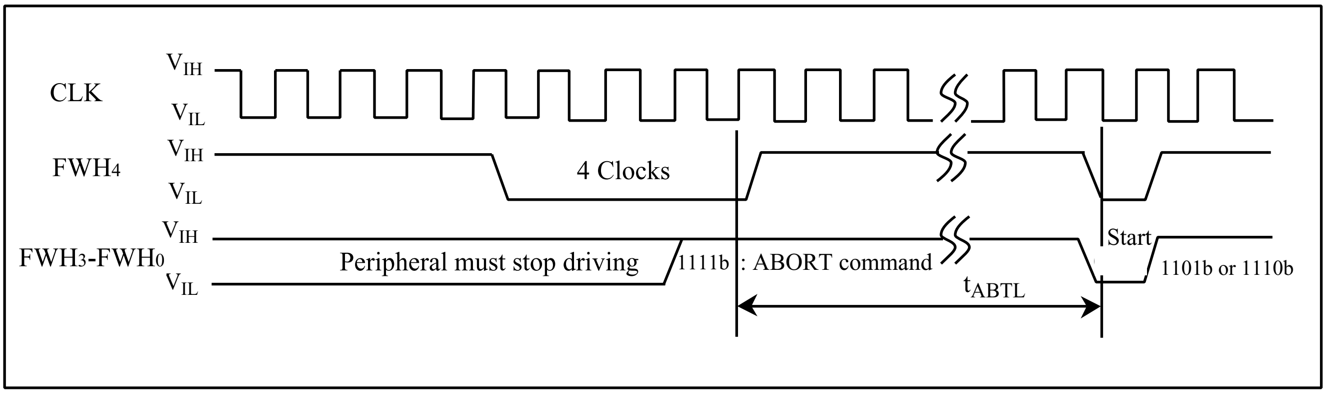


Figure 18. Abort Operation Timing Diagram (FWH Mode)

3.2.6 AC Characteristics (A/A Mode) [1]

Read Characteristics (A/A Mode)

V_{CC}=3.0V~3.6V, T_A=0°C~+85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		250		ns
t_{RSTA}	RST# High Recovery to Row Address		1		µs
t_{AS}	Address Setup to R/C#		50		ns
t_{AH}	Address Hold from R/C#		50		ns
t_{AA}	Address to Output Delay	2		100	ns
t_{OE}	OE# to Output Delay	2		60	ns
t_{OLZ}	OE# to Output in Low Z	3	0		ns
t_{OHZ}	OE# to Output in High Z	3		35	ns
t_{OH}	Output Hold from Address	3	0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed up to $t_{AA} - t_{OE}$ after the rising edge of R/C# without impact to t_{AA}.
3. Sampled, not 100% tested.

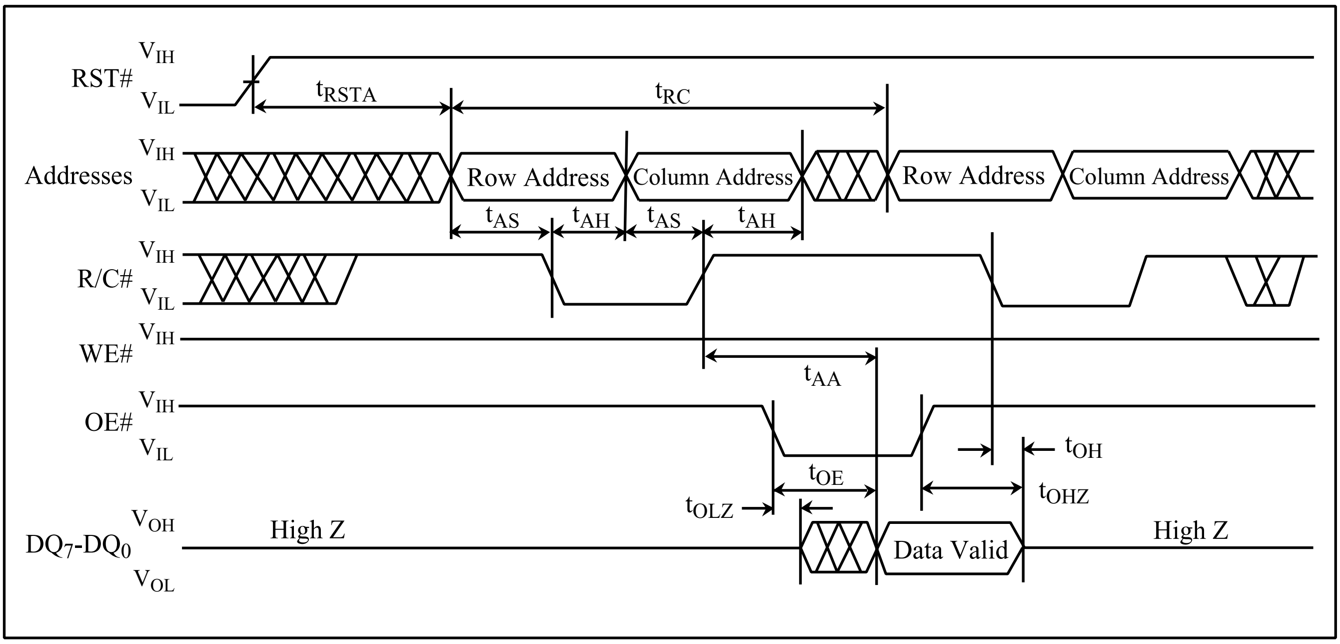


Figure 19. Read Cycle Timing Diagram (A/A Mode)

Write Characteristics (A/A Mode)

V_{CC}=3.0V~3.6V, T_A=0°C~+85°C

Symbol	Parameter	Notes	Min.	Typ.(1)	Max.	Unit
t_{WC}	Write Cycle Time		200			ns
t_{RSTA}	RST# High Recovery to Row Address		30			µs
t_{AS}	Address Setup to R/C#	4	50			ns
t_{AH}	Address Hold from R/C#		50			ns
t_{CWH}	R/C# to WE# High Time		50			ns
t_{OES}	OE# High Setup Time		20			ns
t_{OEH}	OE# High Hold Time		20			ns
t_{OEP}	OE# to Status Polling Delay	2			40	ns
t_{OET}	OE# to Toggle Bit Delay	2			40	ns
t_{WP}	WE# Pulse Width Low		100			ns
t_{WPH}	WE# Pulse Width High		100			ns
t_{DS}	Data Setup to WE# High	4	50			ns
t_{DH}	Data Hold from WE# High		5			ns
t_{IDA}	ID Access Time				150	ns
t_{RB}	WE# High to RY/BY# going Low	3			100	ns
t_{WQV1}	Byte Program Time	3, 5		25	200	µs
t_{WQV2}	Sector Erase Time	3, 5		0.6	5	s
t_{WQV3}	Block Erase Time	3, 5		1.2	6	s
t_{WQV4}	Full Chip Erase Time	3, 5		40	200	s
t_{SWBL}	Set Whole Block Lock Bit Time	3, 5		5	8	µs
t_{CWBL}	Clear Whole Block Lock Bit Time	3, 5		5	8	µs
t_{STBL}	Set Boot Lock Bit Time	3, 5		35	200	µs
t_{CTBL}	Clear Boot Lock Bits Time	3, 5		0.4	1	s

NOTES:
1. Typical values measured at V_{CC}=3.3V and T_A=+25°C. Assumes TBL#, WP# and corresponding lock bits are not set. Subject to change based on device characterization.
2. The timing characteristics for reading the status register during sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits operations are the same as during read-only operations. Refer to Read Characteristics (A/A Mode) for read-only operations.
3. Sampled, not 100% tested.
4. Refer to Table 11 for valid address and data for sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits.
5. Excludes external system-level overhead.

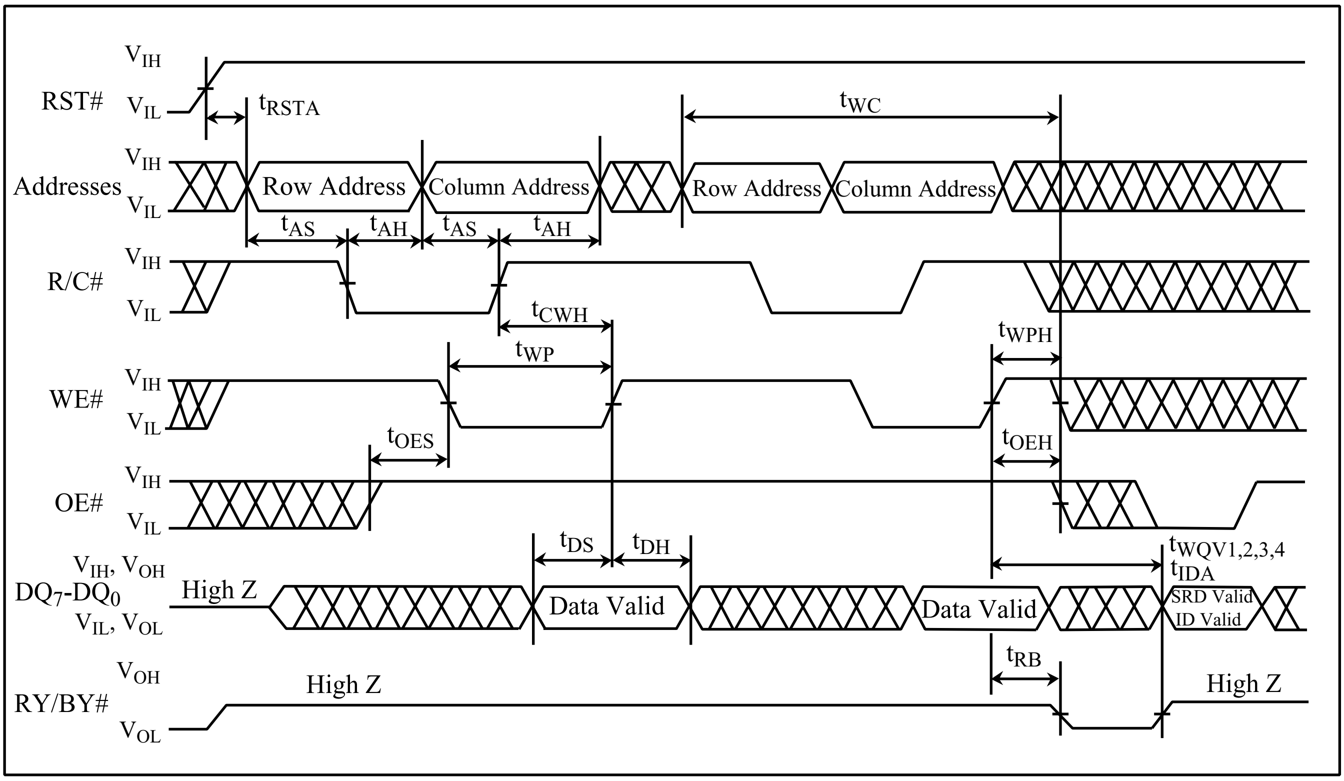


Figure 20. Write Cycle Timing Diagram (A/A Mode)

3.2.7 Reset Operations (A/A Mode)

Reset Characteristics (A/A Mode)

V_{CC}=3.0V~3.6V, T_A=0°C~+85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PRSTH}	V_{CC} 3.0V stable to RST# High	2	100		ns
t_{PRSTL}	V_{CC} 3.0V stable to RST# Low	2	1		ms
t_{RSTP}	RST# Pulse Width Low	1, 2	100		ns
	RST# Slew Rate	2	50		mV/ns
t_{RSTF}	RST# Low to Output in High Z	2		48	ns
t_{RSTA}	RST# High to Row Address Valid	2, 3	1		µs
t_{RSTE}	RST# Low to Reset during erase or program operation	2, 4		30	µs

NOTES:
1. The device may reset if t_{RSTP} < 100ns, but this is not guaranteed.
2. Sampled, not 100% tested.
3. There will be a latency of t_{RSTE} if a reset procedure is performed during an internal operation.
4. If RST# asserted while a sector/block erase, full chip erase, byte program, set whole block lock bit, clear whole block lock bit, set boot lock bit and clear boot lock bits operations are not executing, the reset will complete within 100ns.

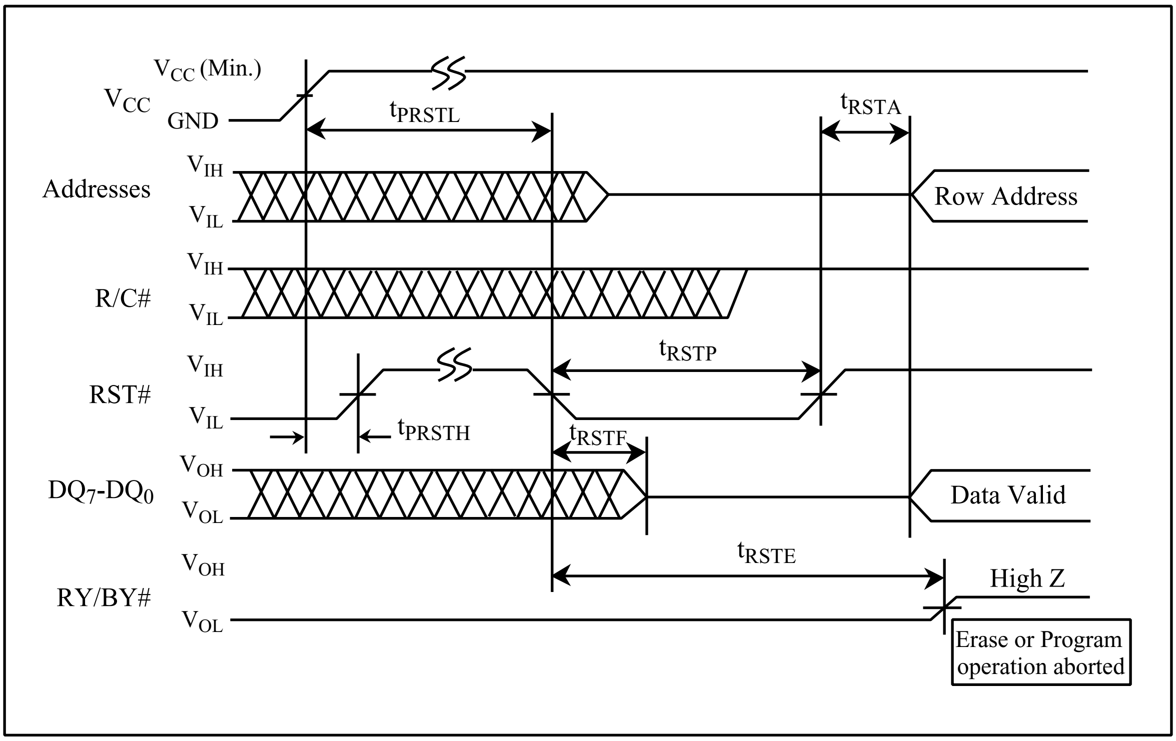
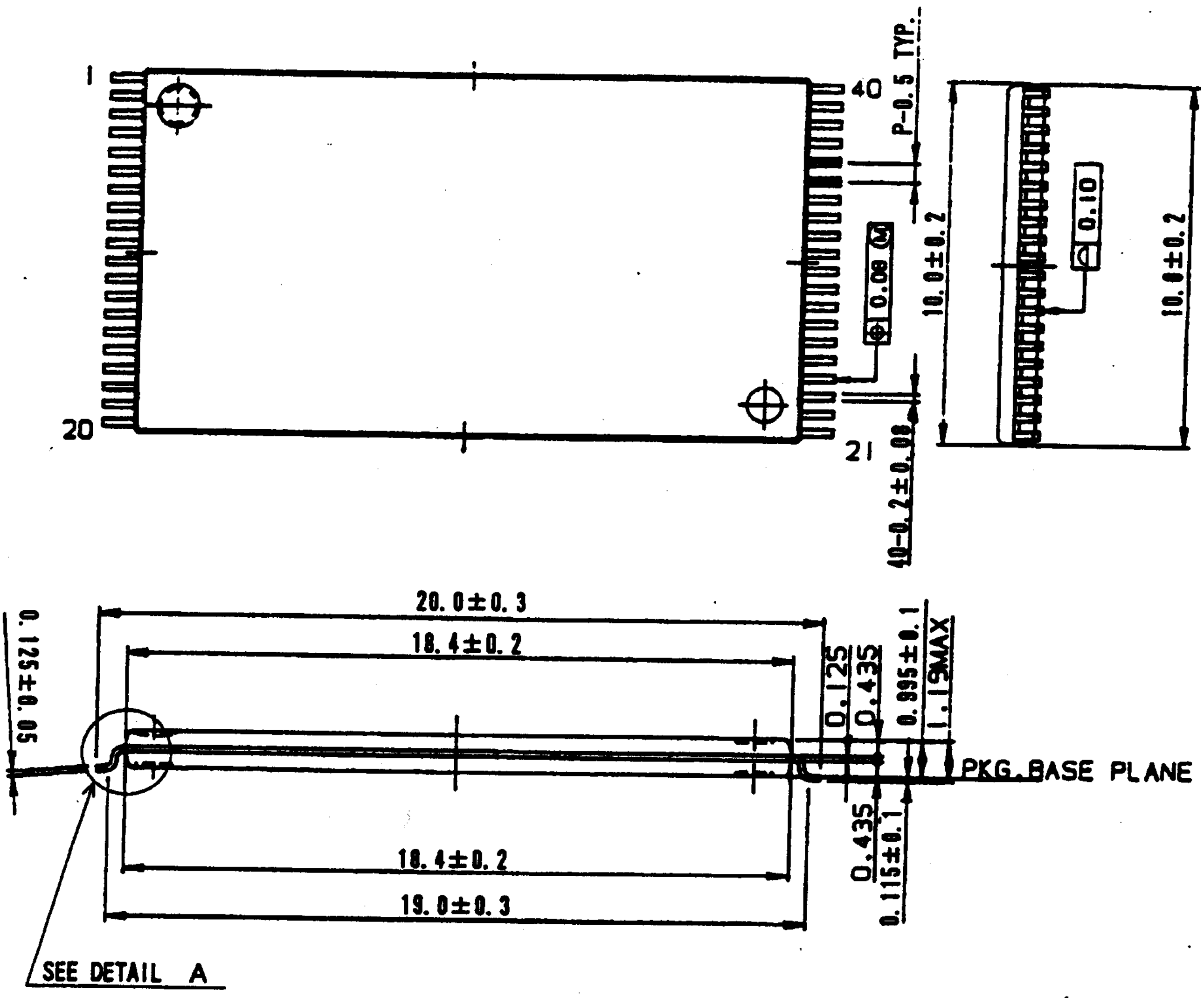
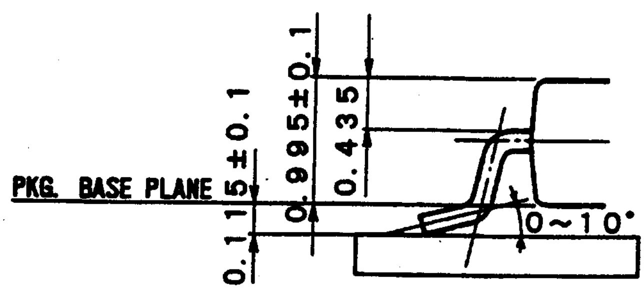


Figure 21. Reset Operation Timing Diagram (A/A Mode)





名称 NAME	TSOP40-P-1020	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE	プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1105	単位 UNIT	mm		

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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